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GLOBAL ELECTRO-THERMAL MODELLING AND CIRCUIT-TYPE SIMULATION OF SIC MOSFET POWER DEVICES IN SHORT-CIRCUIT OPERATION FOR CRITICAL SYSTEM ANALYSIS

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Abstract – The purpose of this paper is to present, for the first time, a global transient electrothermal model and simulation results of commercially recent silicon carbide (SiC) power MOSFET devices. The developed models aim is faithfully transposing specifically experimental short-circuit (SC) behaviour of the studied components, ready-to-use for the analysis of an inverter-leg malfunctioning. After extensive experimentation, a thermal model of the SiC die allows to develop models of gate-leakage current and drain-source current during SC. After verifying the robustness of the proposed models, an original circuit-type with an easy implementation is performed using a commercial circuit simulation tool.

Keywords – electrothermal simulation; model validation; MOSFET; short-circuit; silicon carbide.

1. INTRODUCTİON

Nowadays, due to mass production from major manufacturers, SiC power MOSFET is gradually used in several power applications such as inverter for PV panels and grid, UPS and railway traction drive. In that kind of application, short-circuit (SC) faults can appear leading to large transient power dissipation and a risk of failure. Examples of these faults-types are available on Fig. 1.

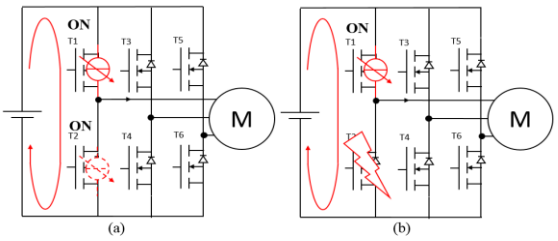


Fig. 1. (a) inverter-leg cross-conduction (Type I SC). (b) Internal short-circuit by electrical breakdown of one of the two leg-switches (Type II SC).

In order to develop a fast and robust protection against these faults, studies on the ruggedness of SiC MOSFET under short-circuit have been carried out [1]–[3]. Nevertheless, none electro-thermal models describe globally and accurately SiC MOSFET behaviour under short-circuit faults. Particularly, the gate-leakage current increases significantly during short-circuit, as depicted in Fig.2, and the saturation current behaviour is unusual compared to silicon (Si) devices. The significant gate-leakage current observed during SC can directly affect the gate-voltage control of the device through the voltage drop across the gate driver resistor. Besides, the temperature-junction estimation in short-circuit mode appears as an important topic to determine the maximum delay time of the gate drive protection circuit.

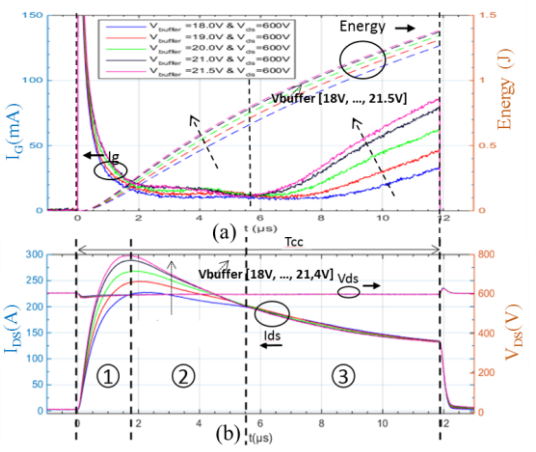


Fig. 2. Experimental waveforms, from a lab. set-up, during SiC MOSFET short-circuit. (a) gate-leakage current and dissipated energy inside the chip. (b) drain current during SC (saturation current) and drain-source voltage.

The goal of the proposed study is to develop a new global and macro-model for SiC MOSFET and particularly applied, in this paper, for the SCT2080KE device from ROHM™. Emphasis has been put on finding and fitting accurate models for transient gate leakage current during SC phase (I_G), drain-source saturation current (I_{Dsat}) and threshold voltage ($V_{GS(th)}$) according to complex and several parameters, particularly using estimated maximum junction temperature (T_j) at the top of the chip. The original contribution of the paper to the classical MOSFET model is highlighted in Fig. 14 at the end of the paper. Combining the gate-current and drain-

source current behaviour, the aim of this paper is to present how the electro-thermal modelling methodology of a SiC MOSFET under extreme stress has been built and evaluated for a practical use. In Section 2, after an introduction, a first dipole-type gate-leakage current model is presented function of four parameters (dissipated energy, gate driver voltage, gate resistance and drain to source voltage). In Section 3, a 1D estimation model of the temperature distribution inside the chip is described. In Section 4, with the results from this estimation, a physical model is fitted in order to simulate the drain-source saturation current evolution during the SC phase. Finally, in Section 5, the simulations of the global behaviour, using PLECS software, are presented and compared with experimentations.

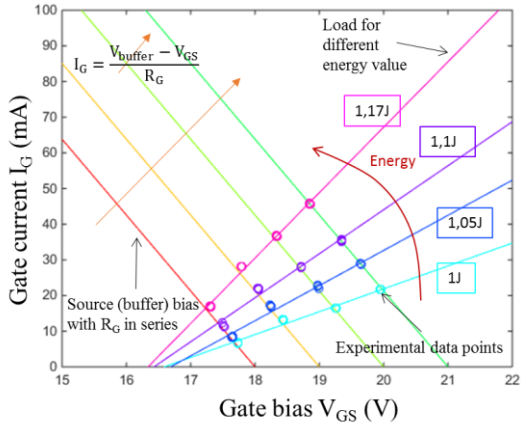


Fig. 3. Measured data points at the intersection between the driver characteristic and the equivalent current-load characteristic F_{IGleak} in the plane (I_G,V_{GS}) for R_G=47Ω, V_{DS}=600V and different dissipated energy values.

2. GATE-LEAKAGE CURRENT MODELLING

2.1. MODEL DETERMİNATİON

After few micro-seconds of short-circuit, a great transient current surge appears across the thin MOSFET gate oxide (50nm). This current is most likely caused by a highly temperature dependant tunnelling considering the important energy dissipated inside the chip (up to 10J/cm² in 12µs). However, the SC duration is much lower than the thermal time constant of the component ($\tau_{die} \cong 350\mu s \gg \tau_{SC} = 12\mu s$). In these conditions, dissipated energy can be considered instead of the junction temperature in order to explain the time dependence of the gate leakage current during SC. Furthermore, as depicted in Fig.2, the gate-leakage current dynamic also depends on the voltage bias imposed by the gate-driver (V_{buffer}), drain-source voltage (V_{DS}) (not displayed) and the external gate resistor (R_G) (not displayed). The aim of this section is to explain how the influence of each parameter has been identified and modelled. In order to reduce the complexity of the study, only gate current increase, along the sequence n°3 in Fig. 3, is modelled. As a result, the surge occurs from a fixed energy (0.8J or 5.9J/cm² of active chip area for all measurements) so the model will be valid from this value only. For the other parameters, the model validity has to be large: $V_{DS} \in [400V,\ 600V]$,$V_{buffer} \in [18V,\ 21.5V]$, $\text{Energy} \in [0.8J, 1.5J]$.

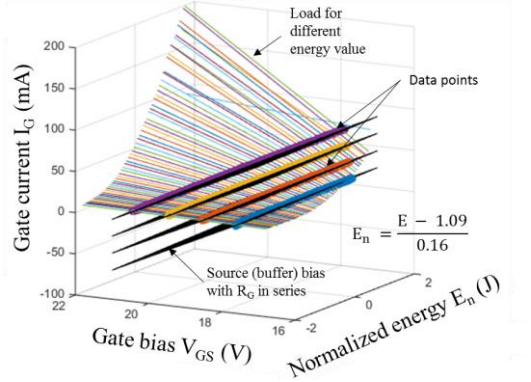


Fig. 4. Measured data points at the intersection between the voltage driver and the current-load characteristic in the space (I_G,V_{GS}, E_n) for R_G=47Ω and V_{DS} =600V.

A "dipole-type" model has been chosen (fig.15) as an equivalent non-linear controlled current-load F_{IGleak} between gate and source electrodes supplied by the driver voltage. This voltage source is made of a voltage source (V_{buffer}) and the series gate resistor (R_G). Only the current-load equation has to be determined. Of course, all experimental data follow source characteristic by a single crossing point (circles in Fig. 3). However, in Fig. 3., it is remarkable that for a given energy and different buffer bias a load straight line is identifiable and is significantly energy (temperature) dependant. In order to analyse the energy influence on the current-load equation, load straight lines are displayed in 3D representation (I_G, V_{GS}, E_n) in Fig.4. This representation is basically the same as depicted in Fig.3. But the load characteristic of the gate driver can be visualised as a surface. Therefore, a polynomial surface (1) has been chosen and fitted with MATLAB™ to model the current-load variation function of V_{GS} and dissipated energy (En) on model validity area.

$$I_g = a_1(E_n).V_{GS} + a_2(E_n) \quad (1)$$

With

$$a_1(E_n) = p_{01} + p_{11}E_n + p_{21}E_n^2 \quad (2)$$

$$a_2(E_n) = p_{00} + p_{10}E_n + p_{20}E_n^2 + p_{30}E_n^3 \quad (3)$$

$(p_{00}, p_{01}, \dots)$ are the estimated factors.

This "response surface" approach has two main advantages. On one hand, MATLAB™ polynomial surface fitting algorithm from the *fit* function is powerful and robust. On an other hand, the polynomial function and dipole type model makes it easily computable and "pluggable" into a commercial-type software. At this point, the model represents effects of $V_{buffer,}$ R_G and E_n on gate leakage current. However, V_{DS} variation is not yet added in

the model. To do that, factors ($p_{00}, p_{01}, \dots$) are, themselves, estimated for different V_{DS} bias and pre-calculated in a table. It appears that these factors are linearly varying with V_{DS}. Then, the variation has been estimated and added to the model.

I. Estimated factors function of V_{ds}

$p00$	$174.2161 - 0.5505.V_{ds}$
$p10$	$192.8417 - 0.5720.V_{ds}$
$p01$	$-11.8436 + 0.0356.V_{ds}$
$p20$	$52.8609 - 0.1482.V_{ds}$
$p11$	$-13.7143 + 0.0386.V_{ds}$
$p30$	$-0.9317 + 0.0026.V_{ds}$
$p21$	$-4.1480 + 0.0111.V_{ds}$

2.2. RESULTS

In order to determine the model robustness, two different tests were made. Firstly, the proposed model was compared with experimental results which are different from those used for the model fitting (Fig.5.(a)). Secondly, the proposed model was compared with data obtained from another component SCH2080KE, i.e. for new experimental results (Fig.5.(b)). The simulation results are, in each case, very close to experimental data. In conclusion, it can be considered that the numerical proposed model is clearly validated and really robust in its full domain of validity.

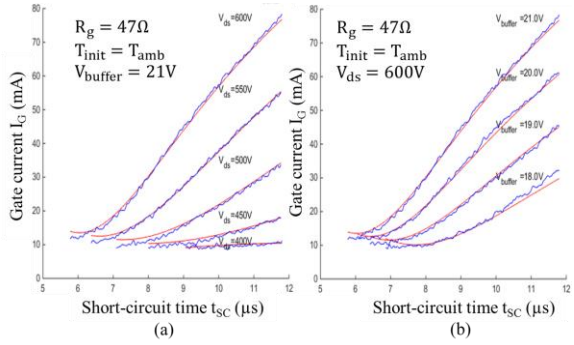


Fig. 5. Model (red lines) and experimental (blue lines) results. (a) robustness results obtained from test data which are not used for the model fitting but with the same device. (b) robustness Results obtained from test data not used for the model fitting and with another device.

3. TEMPERATURE ESTİMATİON

3.1. MODEL CONSTRUCTİON

During a short-circuit event, strong electrical field is distributed along the low doped epi-layer and a strong current density flows through the chip. This particular configuration induces a high and fast transient temperature gradient inside the chip within few micro seconds. With encapsulated components, the temperature gradient is not measurable in real time because the external case temperature do not represent the junction temperature of the chip [4]. In order to fit physical models, such as temperature dependant electron mobility or threshold voltage, an accurate temperature estimation is needed. All these physical models are required for the drain – source current proposed model. Moreover, the thermal model must be accurate and low simulation time consuming. To do that, the best compromise is a one dimensional transient thermal model across the chip depth, as shown in Fig. 6.

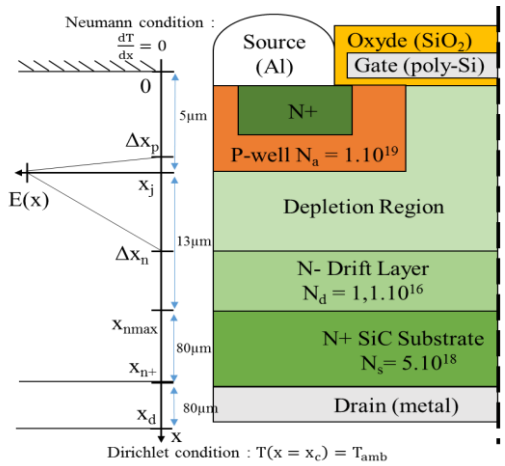


Fig. 6. 1D thermal model of the SiC MOSFET.

During short-circuit transient, the dc bus voltage, V_{DC}, is applied across the power device and leads to a depletion layers with a width x_p in the P-well (highly doped N_a) and x_n in the N-drift region (low doped N_d). The resulting electric-field distribution in the space charge region is given by [2], neglecting the effect of the current on the depleted charges.

for: $x_p \le x \le x_j$

$$E(x) = \frac{qN_a}{\epsilon_s}\left(x + \Delta x_p - x_j\right) \quad (4)$$

for : $x_j \le x \le x_n$

$$E(x) = -\frac{qN_d}{\epsilon_s}\left(x - \Delta x_n - x_j\right) \quad (5)$$

for : $x \le x_p$ and for $x \ge x_n$

$$E(x) = 0 \quad (6)$$

Where ϵ_s is the dielectric constant for 4H-SiC material and q is the electron charge. V_{DS} is the electric field integral along the space dimension.

$$V_{ds} = \frac{E(x_j)\cdot \Delta x_n}{2} + \frac{E(x_j)\cdot \Delta x_p}{2} \quad (7)$$

Doping values and dimensions in Fig 6. are chosen according to the literature data [5]. It results a $\Delta x_n = 7.6\mu m$ and $\Delta x_p = 8nm$ at V_{DS}=600V.

The 1D approximation of the heat flux profile in the volume $Q(x, t)$ [W/m^3] is depending on the electric field [V/m] function of the variable "x" and the drain-saturation current function of the variable "t" with the following formulation:

$$Q(x,t) = \frac{E(x)\cdot I_{DS}(t)}{S_{chip}} \quad (8)$$

Where $I_{ds}(t)$ is the experimental short-circuit current and S_{chip} ($13.6mm^2$) the active chip area.

Fig.6 depicts the boundary conditions. The top surface of the chip is assumed adiabatic due to the thick plastic coating around the die and the bottom is considered at a constant temperature (ambient temperature) due to the fact that the heat diffusion depth is much lower than the thickness of the die at the end of the short-circuit stress and has been confirmed by changing the boundary conditions (not presented here). This 1D model is implemented with COMSOL® software.

3.2. RESULTS

In fig. 7 and 8, $T_j(x,t)$ the temperature distribution in the die and the maximum temperature are presented function of the short circuit duration. Estimated temperature increases up to 1300K for 12µs of SC duration. Estimated temperature are representative to results already observed in the literature [2], [6] but obtained with other estimation methods which tend to confirm the results. Moreover, temperature is maximal for $x=x_j$ where the electrical field is also maximum. For the following thermal modelling, only the maximum estimated temperature will be used.

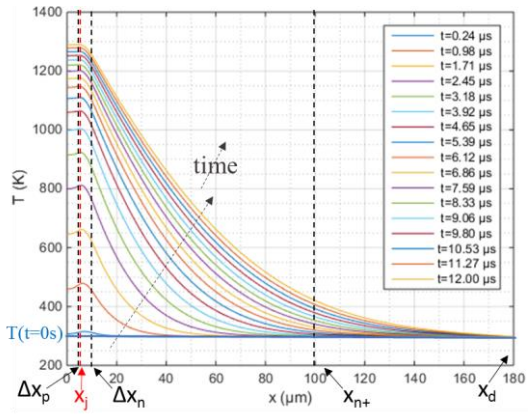


Fig. 7. Estimated T(x, t) temperature distribution vertically along the component for a short-circuit at V_{ds}=600V, V_{buffer}=21V, T_{init} (t=0)=298,15K.

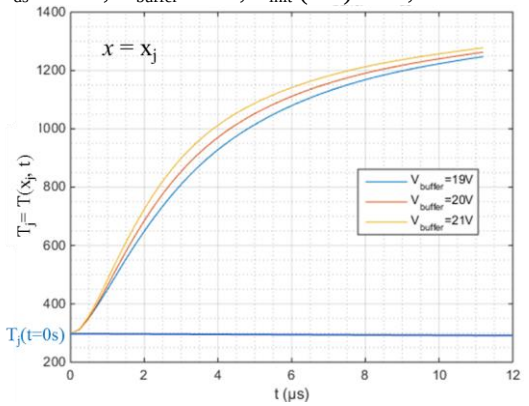


Fig. 8. 1D Estimation of the maximum junction temperature T_j (x_j, t) for different buffer-voltages bias at V_{ds}=600V, T_{jinit} (t=0s)=298,15K.

4. DRAİN-SOURCE CURRENT MODELLİNG

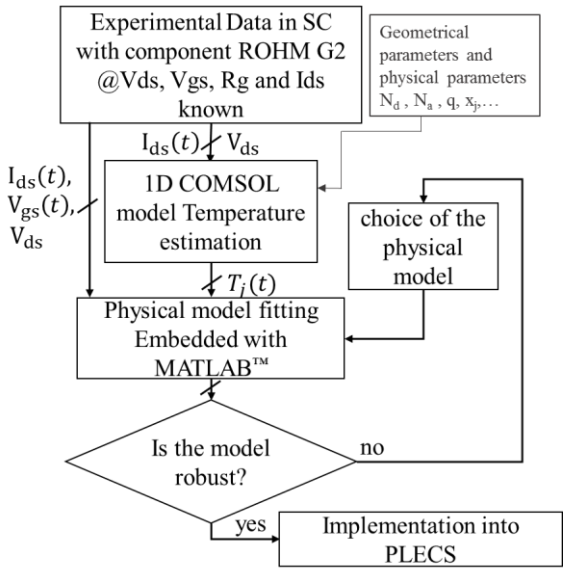


Fig. 9. Saturation current determination methodology

To accurately model the drain-source saturation current as it is shown in Fig. 2b, a representative physical model is needed. Available models depend of a lot of physical parameters that are not known over a wide temperature range. In order to estimate them, data from experiment are needed. Methodology is summarized in Fig. 9. Different models have been tested but finally, the following model has been chosen due to its classical form [7]:

$$I_{Dsat}(T_j) = \frac{K_{gm}(T_j)}{2} \cdot \left(V_{gs} - V_{gs(th)}(T_j)\right)^2 \quad (9)$$

With

$$K_{gm}(T_j) = \frac{\mu_n(T_j) \cdot C_{ox} \cdot Z}{L} \quad (10)$$

Where, C_{ox} is the oxyde capacitance, Z and L are the width and length of the channel respectively. The carrier mobility in the channel, μ_n, is at least the parallel combinations of three different mobility functions with different sensitivity toward temperature [8]. The Matheissen's rule gives:

$$\mu_n(T_j) = \frac{\mu_{a0}\left(\frac{T_j}{T_0}\right)^a}{1 + \frac{\mu_{a0}}{\mu_{b0}}\left(\frac{T_j}{T_0}\right)^{b-a} + \frac{\mu_{a0}}{\mu_{c0}}\left(\frac{T_j}{T_0}\right)^{c-a}} \quad (11)$$

Where μ_{a0}, μ_{b0}, μ_{c0} are mobility parameters at ambient temperature and a,b,c are sensitive thermal coefficients that have to be estimated to obtain a wide range temperature model. Otherwise, literature [7], gives a linear threshold voltage dependence with temperature:

$$V_{gs(th)}(T_j) = x_1 \cdot T_j + x_2 \quad (12)$$

Where x_1 and x_2 are unknown parameters. All the previous parameters are determined in two steps. At first, K_{gm} and $V_{gs(th)}$ are determined function of the temperature. To do that, an algorithm has been developed to find the best pair of parameters (x_1, x_2)

which minimize the difference between calculated K_{gm} with the equation (9) for different experimental data. Results are displayed in Fig. 10, with the couple (x_1=-0.025, x_2=15.4) and K_{gm} remain the same for different buffer bias (19V, 20V, 21V). In a second time, the mobility model (11) is fitted on K_{gm} profile previously determined using MATLAB's function *fit*. Results are evaluated in Fig.11.

Unfortunately, the model is not robust to V_{ds} variation. Other models have been tested to take this parameter into account but without success. The next step is to take into account a more complex model and use a metaheuristic method, such as genetic algorithm, to find the optimum and to precisely take into account variation of the DC bus voltage.

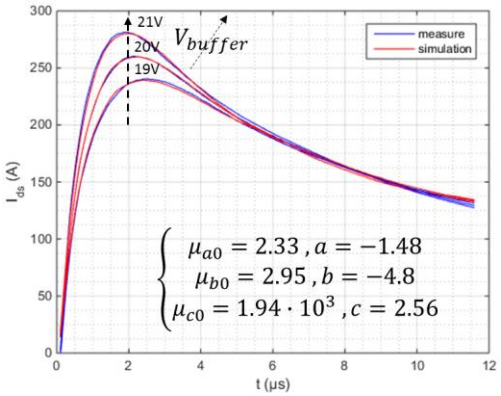


Fig. 11. Saturation current results obtained after fitting for different gate bias (experimental results in blue lines and simulation results in red lines).

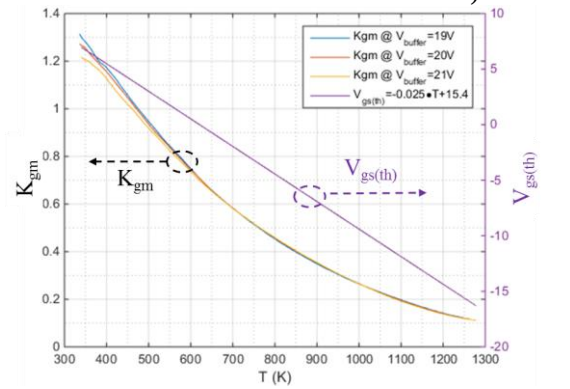


Fig. 10. K_{gm} and $V_{gs(th)}$ fitting based on the 1D thermal model and experimental data acquired with different gate bias and V_{DS}=600V.

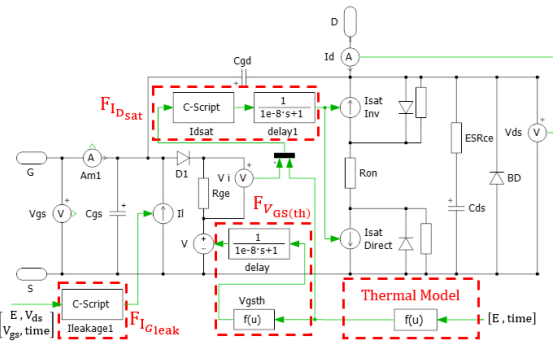


Fig. 12. Proposed SiC MOSFET model in PLECS software.

5. IMPLEMENTATION IN PLECS

The models have been implemented in PLECS™, a software for simulations of electrical circuits. PLECS presents the advantages of being easily pluggable with MATLAB and of quickly simulating complex topologies. The aim of this section is to present all the previous results implemented into a single circuit-type model as summarized in Fig.14.

The classical MOSFET model (in Fig.14 black line) is completed (in red line) adding the previous gate leakage current modelling by "F_{IGleak}", the drain-source current modelling by "F_{Idsat}" and finally the gate threshold voltage by "F_{VGth}". The different models are performed by PLECS function block or by code-C script. The PLECS schematic is displayed in Fig.12. Today, the co-simulation between COMSOL and PLECS has not been implemented. In order to estimate the junction temperature inside the chip without COMSOL the following simplified model is proposed based from [9]:

$$\Delta T_j(t) \cong \frac{K}{S.\rho.c.\sqrt{\pi.\alpha}} \frac{1}{\sqrt{t}} \int_0^t P(\tau)\, d\tau \qquad (13)$$

Where ρ is the density of the SiC material (kg.m^{-3}), S is the chip area (m^2), $P(t)$ is the power dissipated into the chip (W), c the specific heat of SiC (J.Kg^{-1}.K^{-1}), α the thermal diffusivity of SiC (m².s^{-1}) and K is a dimensionless corrective factor. By fitting K factor, we show that this simple model can give results close to those obtained by the COMSOL model.

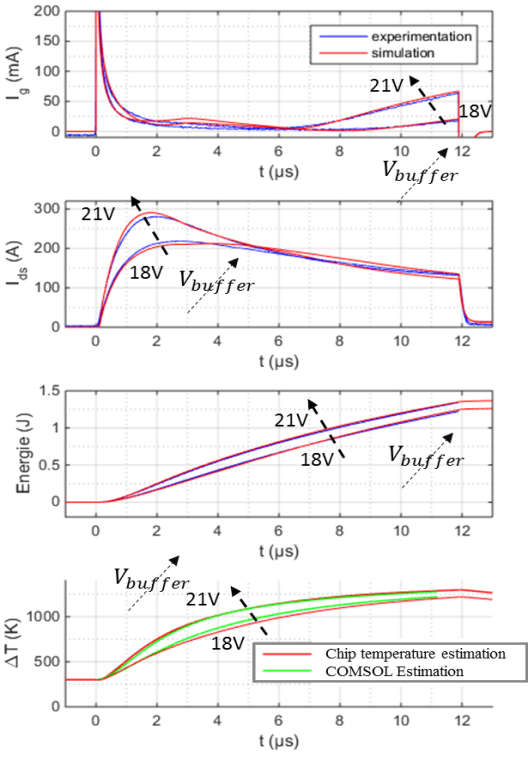


Fig. 13. Simulated waveforms from the proposed PLECS circuit-type model compared with measured ones for different buffer voltages bias (@Vds=600V, Tj_{init}=298,15K (25°C) and Rg = 47Ω)

The results of the whole simulation are shown in Fig.13. Our objective is fulfil: the simulation is well working and will be able to be used in more complex circuit, for example, short-circuit detection and more generally concerning the safety analysis of critical system. Moreover, the model clearly represent the effect of the buffer voltage bias variation. All the modelling procedure is automatized in MATLAB and this model could be easily obtained for other SiC MOSFET components. However, strong coupling with PLECS circuit and COMSOL 1D model should be implemented and drain saturation current robustness to V_{DS} voltage variation has to be also investigated in future works.

6. Conclusion

The aim of this paper was presenting a complete and new modelling methodology for SiC power MOSFET device in high-current and high-temperature conditions. Firstly, the gate transient leakage current is modelled. In a second step the temperature is estimated inside the chip and finally a physical model of the drain saturation current is given. After validating these different models all the previous models are embedded into a circuit-type MOSFET model. This "block" could be used, as it is, to simulate fault into complex circuits using SiC MOSFET components like a motor drive, for example. Moreover, the proposed model enhancement does not add lot of calculation time and is fully compatible with classical numerical or circuit-type MOSFET models. Results are presented for the ROHM component SCT2080KE but the method is clearly practical for other manufacturers such as CREE or STMicroletronics.

Acknowledgements

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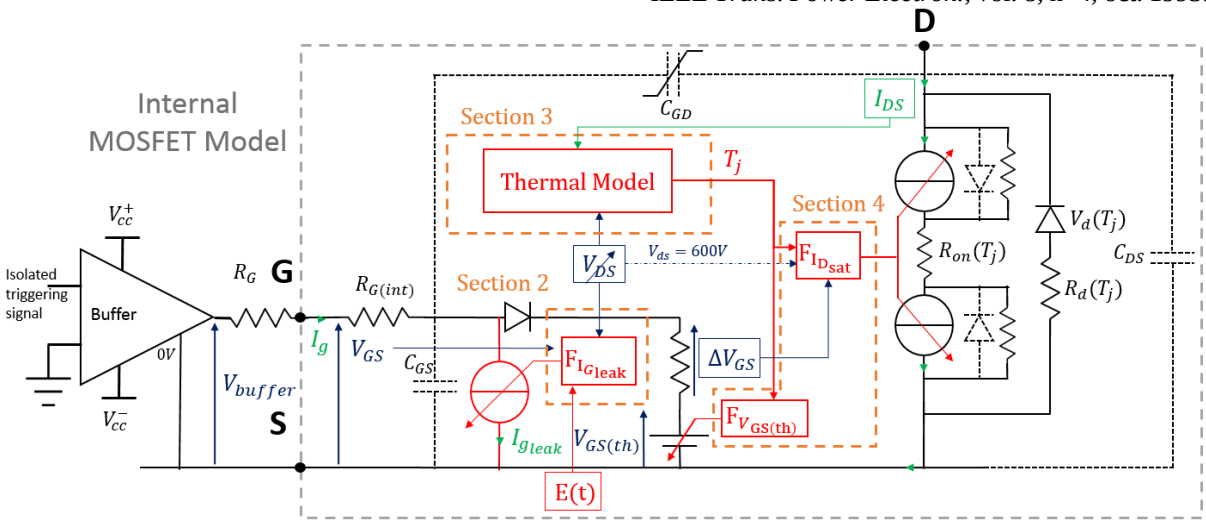


Fig. 14. Enhanced electro-thermal SiC MOSFET model. In black line, the classical MOSFET model. In red line, features proposed in this article.