

In-depth investigation of metallization aging in power MOSFETs

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Abstract

The long-term reliability of modern power MOSFETs is assessed through accelerated electro-thermal aging tests. Previous studies have shown that the source metallization (top metal and wires) is a failure-prone location of the component. To study how the top Aluminum metallization microstructure ages, we have performed ion and electron microscopy and mapped the grain structure before and after avalanche and short-circuit aging tests. The situation under the bond wires is significantly different as the bonding process induces plastic deformation prior to aging. Ion microscopy seems to show two inverse tendencies: grain growth under the wires and grain refinement elsewhere in the metallization. Transmission electron microscopy shows that the situation is more complex. Rearrangement of the initial defect and grain structure happen below and away from the wire. The most harmful fatigue cracks propagate parallel to the wire/metal bonding interface.

1. Introduction

Power MOSFETs-based devices in the automotive industry have evolved beyond their initial electrical switch function as they integrate now several auto-diagnosis capabilities. At the same time, a better control of the fabrication process, materials purity and defect structure significantly improved their reliability. However, some parts of power components remain prone to electrical and/or thermo-mechanical aging and are thus critical for reliability assessment.

These parts have been identified as the metallic ones such as the die attach (where alternatives to lead-based solder are emerging [1,2]), and the source metallization, including the top metal and the bond wires attached to it [3-6]. The plastic deformation of the source metallization and wire bonds is linked to the difference in the coefficient of thermal expansion (CTE) between the Silicon (Si) chip and the metallic parts. Since Aluminum (Al) has a low elastic limit, the source metallization is expected to deform even for moderate temperature excursions (200°C). Cu-based metallizations experience similar degradations [7] but seem to have a better overall endurance [8]. Deformations of the source metal have a clear impact on the drain-source resistance ($R_{ds(on)}$), which increases over cycles. In turn, this resistance augmentation leads to larger thermal gradients.

In a previous study [9,10], we have shown that most of the metallization degradations during aging could be the result of intergranular diffusion and surface reconstruction. This scenario [11] is however confronted to the fact that temperature cycles in a MOSFET are very abrupt and thus favor a dislocation-based plastic deformation.

Here, we follow the evolution of the microstructure of the Aluminum-based source metallization of power MOSFETs, during accelerated aging tests. We focus on the grain and grain boundary structure of the source layer away and just under the wire bonds. This buried zone is prone to failures [4] but its fine microstructural characterization has proven complicated to perform so far. Here, we have used ion milling and microscopy, coupled with transmission electron microscopy, to map and quantitatively measure the microstructure aging in a MOSFET undergoing accelerated tests at these key locations.

2. Experimental

2.1. DUT and accelerated aging tests

The device under test (DUT) is a 24V Freescale's SmartMOS technology dedicated to truck application. The active zone is made of 2 MOS sectors, each connected by 3 Al wedge bond wires (Fig. 1). During the tests, only one sector is undergoing repeated electrical pulses, either in avalanche or short-circuit mode (energy density in the order of $3\text{J}/\text{cm}^2$ for each test). Avalanche tests seem to induce a slower aging compared to short-circuits, but more data is needed to verify this point. Electrical wave forms (current, voltage and power) recorded during tests are depicted in figure 2. During the short-circuit phase (600A at the beginning) the high current level induces a high power dissipation.

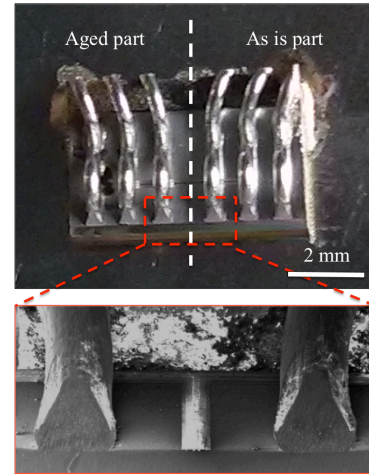


Fig. 1. Power module prepared for microstructural inspection after aging. The left sector is aged (avalanche mode, 400 kcycles) as the right one is as processed. The wires are cut and polished to 45° before being FIB-cut for interface observation.

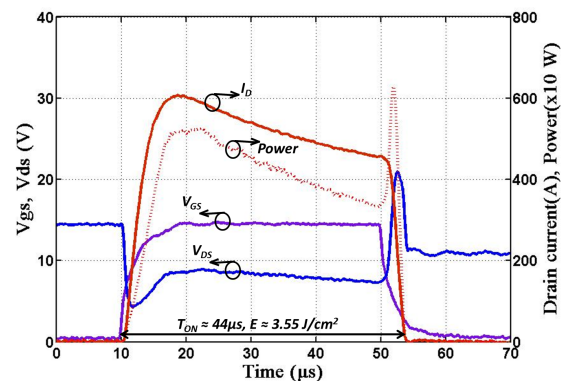


Fig. 2 : Drain current, drain-to-source voltage and dissipated power during short-circuit phase, $V_{DS}=15\text{V}$, $V_{GS}=15\text{V}$, $T_{on}=44\mu\text{s}$.

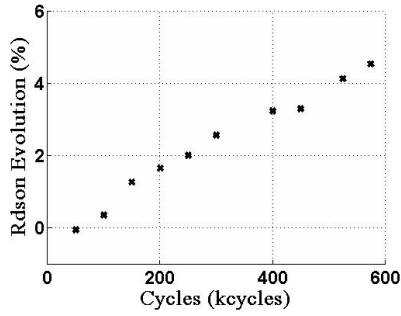


Fig. 3: On state resistance increase during repetitive short circuit tests, $V_{DS}=15V$, $V_{GS} = 15V$, $T_{on} = 44\mu s$.

R_{dson} linearly increases during short circuit aging (Fig. 3). During these tests, the aging of Aluminum surface has been monitored at various stages (1k, 2k, 10k, 100k, 600k cycles) using SEM (Scanning Electron Microscopy).

2.2. Microstructural characterization

Surface observation and EBSD (Electron Back Scattered Diffraction) mapping were performed in a Helios 600 FIB/SEM. Figure 4 shows a weak change in the Al surface starting from 10k cycles, but it is only after 100k cycle that we observe a significant increase of the roughness.

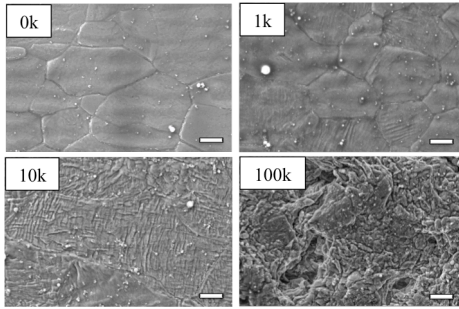


Fig. 4. SEM observation of the metallization surface after 0, 1k, 10k and 100k cycles. Scale bar 2.5 μm .

However, observation of the in-depth structure of the metallization and of the interface under the bond wires requires making cross sectional cuts of the device. This is done through both mechanical grinding (made at 45° of the surface, see Fig. 1, to let access to the ion beam) and Focused Ion Beam (FIB) cross-sectional cuts, performed perpendicular to the surface. These cross-sections are first observed using ionic channeling contrast (Fig. 5), which depends on grain orientation. This gives a first idea of the grain

size (measured by the line intercept method [12]) in both the source metallization and the bond wire. It also allows measuring the deformation imposed to the initial Al layer by the wire bonding process and seeing how this interface behaves during aging.

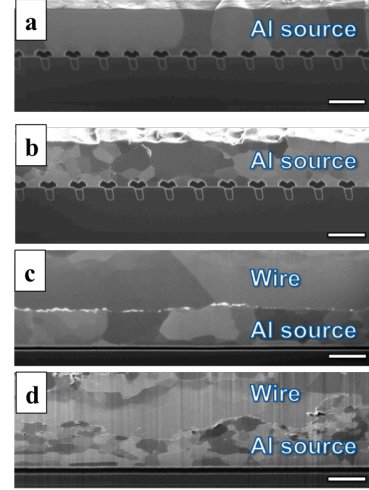


Fig. 5. FIB imaging of the naked metallization in an a) as-is and b) aged power module and of the wire-source metallization interface in an c) as-is and d) aged power module.

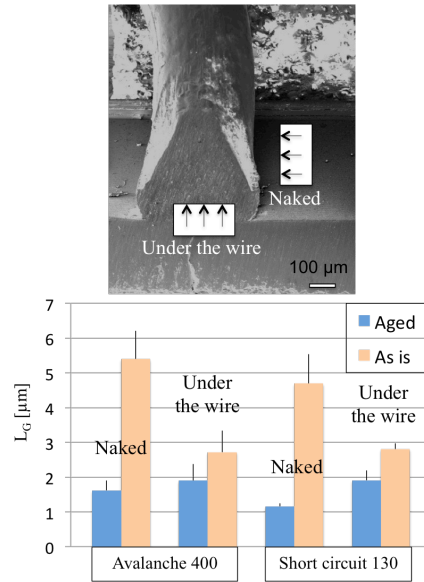


Fig. 6. Sketch of the two locations where FIB cross-sections are made (the arrows indicate the analyzed surface). The plot represents the grain size, measured by the linear intercept method [12], in the metallization both under the bonding wire and outside (naked) for as-is and aged modules in avalanche (400 kcycles) and short circuit (130 kcycles) mode.

A TEM-lamella (Fig. 8) of the same zone is then prepared by removing matter behind the observed zone using the ion beam, lifting out the lamella and thinning it down to electron transparency with decreasing flux of ions (Fig. 7).

TEM observations are performed in a JEOL 2010 and in a Philips™ CM20FEG equipped with a Digistar™ –ACOM (Automated Crystal Orientation Mapping) unit from NanoMEGAS™. This system captures the diffraction patterns of a given zone and returns the crystallographic orientation of each scanned point to build orientation maps of TEM samples as in Fig. 10b. EBSD and ACOM methods are complementary as they give surface or in depth information, respectively.

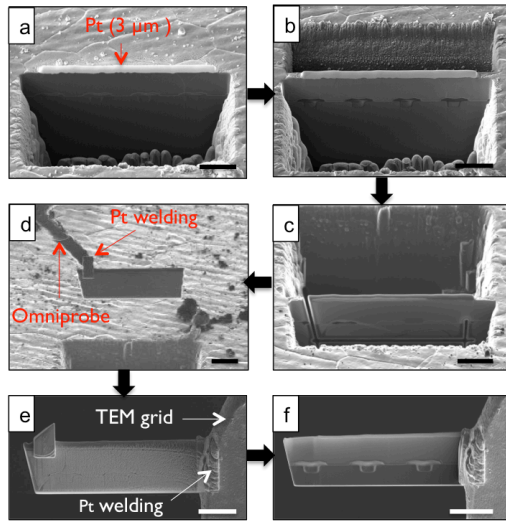


Fig. 7. Cartoon of a typical TEM-lamella preparation by FIB: *a)* deposition of a protective Platinum (Pt) layer on the area of interest, and *b)* matter removal behind the lamellae; *c)* cutting of lamella; *d)* lamella welding and lift out by Omniprobe; *e)* welding of lamella on TEM grid; *f)* final thinning and polishing. Scale bar 5 μm .

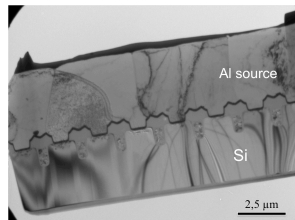


Fig. 8. Bright field TEM imaging of a FIB-prepared lamella from an as-is sample.

3. Results

3.1. Al metallization

Outside of the wire bonding area, the initial grain size is on the order or larger than the metallization thickness. The structure is called "bamboo" as most of the grain boundaries run perpendicular to the surface down to the substrate. An EBSD map of the initial metallization surface reveals a strong $\langle 111 \rangle$ texture (Fig. 9a) that is confirmed by a TEM cross section oriented through ACOM (Fig. 9b). This last image clearly shows that each grain orientation is conserved from the surface down to the transistor region.

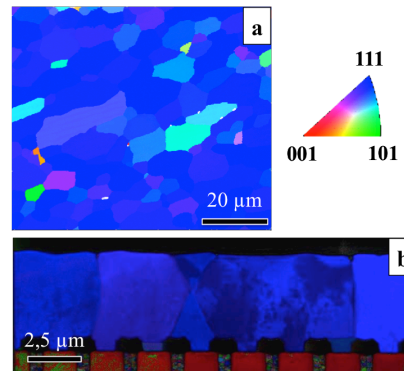


Fig. 9. EBSD mapping of *a)* the surface and *b)* the cross-section of an as is module, showing a strong 111 texture of the Al grains along the deposition direction.

Aging seems to lower the average grain size (as measured by FIB in Fig 6 and observed elsewhere [13]), but ACOM mapping shows that most of the grain domains revealed by FIB have a small misorientation (less than 10°). Fig 10 illustrates this as two grains (1 and 2) visible in ionic contrast (Fig. 10a) have only a 8° misorientation when measured using the ACOM system (Fig. 10b). These are then subgrains potentially formed by the gathering of initial dislocations inside a single initially large bamboo grain [10]. Many cracks running from the surface to the Si substrate are observed (Fig. 10). They follow the grain boundaries and are probably the signature of a heavy Al self-diffusion process between the grains [10].

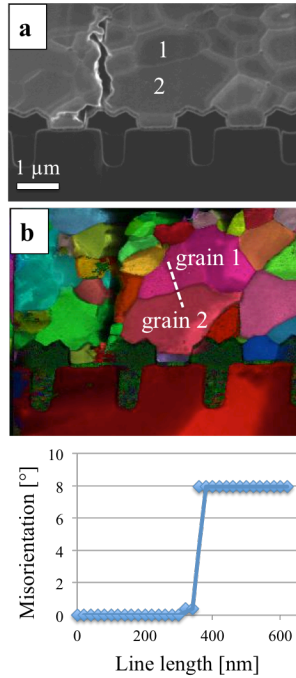


Fig. 10. a) FIB imaging and b) ACOM orientation mapping of the source metal of an aged module (short circuit, 130k cycles) at the interface with the Si substrate. The plot represents the misorientation between the grains 1 and 2 along the white line in b).

3.2. Al metallization under the wire bondings

Under the wire, the Al metallization is severely deformed, with plastic deformation ranging from 5 to 25%, in average, in the measured sections. The deformation is measured by taking the initial metallization thickness (away from the wire) in a non aged device as reference. The grain size is systematically smaller in these zones, as it can be seen in Fig. 6 and Fig. 11. In this figure, one can also note that grains in the Al wire are much larger. Upon aging, the amount of plastic deformation perpendicular to the interface does not change significantly, but grain growth is observed, at variance with what happens outside the wire-bonding area. The initial dislocation density is also higher in this zone, which forecasts larger rearrangements, cell formations and subsequent grain boundaries creation. The bonding between the metallization and the wire shows initial imperfections, probably due to Al oxide (visible in white contrast in Fig. 2). Cracks propagate along these imperfections during aging, causing a loss of contact (or a reduced contact area) between the wires and the metallization. This mechanism, coupled with cracks running perpendicularly to the

interface (under and away from the bondings) must cause a R_{dson} increase. This R_{dson} increase implies that subsequent electrical pulses will generate more heat, thus more deformation, and crack propagation. The linear character of the resistance increase is however not linked yet to a total crack surface measurement that is unavailable so far.

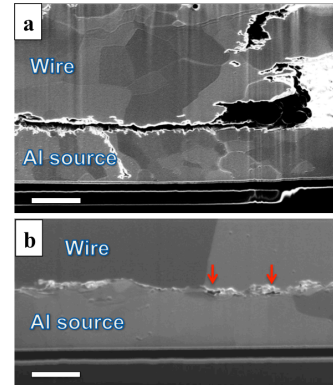


Fig. 11. FIB imaging of the wire-source metallization interface in an aged power module (short circuit 130 keycycles) at a) the edge and b) in the middle of the wire. Scale bar 2.5 μm.

4. Conclusion

Systematic observations of the Al-based source metallization of power MOSFETs, that underwent accelerated electro-thermal tests, revealed that aging occurs through a change in the Al grain microstructure. Under the wire bondings, the initial microstructure is much finer than elsewhere and a strong grain growth is observed. Away from the wire bonds, the metallization undergoes an apparent but limited grain growth. Cracks are observed to run perpendicular to the surface down to the substrate in bare metallization regions (following the grain boundaries), while they also propagate along the wire-metallization interface under the bondings. These mechanisms are probably linked to an enhanced self-diffusion of Al atoms along the boundaries and to a poor bonding of the wires due to the presence of Al oxide that is not fully broken during the bonding process. Both mechanisms explain why the R_{dson} increases during electro-thermal aging.

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References

- [1] Caccuri V, Milhet X, Gadaud P, Bertheau D, Gerland M. *Journal of Electronic Materials* 2014;43:4510–4.
- [2] Le Henaff F, Azzopardi S, Deletage JY, Woïrgard E, Bontemps S, Joguet J. *Microelectronics Reliability* 2012;52:2321–5.
- [3] Irace A, Breglio G, Spirito P, Letor R, Russo S. *Microelectronics and Reliability* 2005;45:1706.
- [4] Glavanovics M, Detzel T, Weber K. *Proceedings of the 34th European Solid-State Device Research Conference, 2004*, pp. 273–6.
- [5] Pietranico S, Lefebvre S, Pommier S, Berkani Bouaroudj M, Bontemps S. *Microelectronics Reliability* 2011;51:1824–9.
- [6] Ciappa M. *Microelectronics Reliability* 2002;42:653–67.
- [7] Nelhiebel M, Illing R, Detzel T, Wöhlert S, Auer B, Lanzerstorfer S, et al. *Microelectronics Reliability* 2013;53:1745–9.
- [8] Nelhiebel M, Illing R, Schreiber C, Wöhlert S, Lanzerstorfer S, Ladurner M, et al. *Microelectronics Reliability* 2011;51:1927–32.
- [9] Martineau D, Mazeaud T, Legros M, Dupuy P, Levade C, Vanderschaeve G. *Microelectronics and Reliability* 2009;49:1330–3.
- [10] Martineau D, Levade C, Legros M, Dupuy P. *Microelectronics Reliability* 2014;54:2432–9.
- [11] Martineau D, Mazeaud T, Legros M, Dupuy P, Levade C. *Microelectronics Reliability* 2010;50:1768–72.
- [12] Tomkeieff SI. *Nature* 1945;155:24–4.
- [13] Bernoux B, Escoffier R, Jalbaud P, Dorkel JM. *Microelectronics Reliability* 2009;49:1341–5.